REMARKS

Applicant's counsel thanks the Examiner for the careful consideration given the application. Claims 1 to 30 are presently pending in the application. Claims 1, 14, 16, 17, 19, 20, 21, 22, 23 and 24 have been amended to more clearly and precisely define the present invention.

The Examiner rejected claims 1-23 under 35 USC 102(e) as being anticipated by Wu et al (US 6,111,245).

Wu discloses a basic CMOS active pixel sensor (APS) (see figure 3 and col. 2, lines 17 to 57), of the type that can be operated in a "correlated double sampling" manner and which can be used in a conventional image sensor array having rows and columns (see figure 2 and col. 2, lines 9 to 16). Wu further discloses a method of reducing the overall power consumption of each APS by using a PMOS transistor M2 as the reset transistor, which is operable at lower voltages due to the body effect (ie: PMOS transistors operate at lower voltages) (col. 3, lines 13 to 23). Wu's method allows for the operation of the imaging array at voltages of less than 2 volts. It is to be noted that Wu achieves power conservation on an individual APS basis.

The present invention is directed to a CMOS active pixel sensor (APS) transducer array having a number of APS's arranged in columns and rows for sensing an image, wherein the array is adapted to decimate the image by accessing output signals only from selected APS's. The power consumption of the APS array is controlled by connecting only the selected APS's between a power supply terminal and a ground terminal. The balance of the APS's, i.e. those that are not accessed to form the decimated image, are not energized, thus reducing the power consumption of the APS array.

Wu does not discuss an image decimation technique, and further Wu does not teach a circuit that can connect and disconnect APS's from between

a power supply and ground thereby deenergizing selected APS's during the imaging process.

Specifically, Wu does not teach:

- "means for connecting the **selected** APS's between the power terminal means and the ground terminal means" (emphasis added) as defined by claim 1;
- "means for coupling the APS's between the power terminal and the ground terminal comprising N transistor means wherein each of the N transistor means is connected between APS's in a respective column and the power terminal, and further coupling means for coupling the APS's in the respective columns to the ground terminal." as defined in claim 14;
- "means for coupling the APS's between the power terminal and the ground terminal comprising N transistor means wherein each of the N transistor means is connected between APS's in a respective column and the ground terminal, and further coupling means for coupling the APS's in the respective columns to the power terminal." as defined by claim 17;
- "means for coupling the APS's between the power terminal and the ground terminal comprising M transistor means wherein each of the M transistor means is connected between APS's in a respective row and the power terminal, and further coupling means for coupling the APS's in the respective row to the ground terminal." as defined in claim 20; and
- "means for coupling the APS's between the power terminal and the ground terminal comprising M transistor means wherein each of the M transistor means is connected between APS's in a respective row and the ground terminal, and further coupling means for coupling the APS's in the respective row to the ground terminal." as defined by claim 22.

Claims 2 to 13, which are directly or indirectly dependent on claim 1, further define the connecting means and the location of the selected APS's. These limitations are not taught by Wu.

Claims 15, 16, 18, 19, 21 and 23, which are directly or indirectly dependent on claims 14, 17, 20 and 22 respectively, define the coupling means and control means. These limitations are not taught by Wu.

It is therefore respectfully submitted that Wu does not anticipate present independent claims 1, 14, 17, 20 and 22, and the Examiner is respectfully requested to withdraw his rejection of these claims as well as dependent claims 2 to 13, 15, 16, 18, 19, 21 and 23 under 35 USC 102(e) as being anticipated by Wu.

The Examiner rejected claims 24-30 under 35 USC 103(a) as being unpatentable over Wu et al (US 6,111,245) in view of Lee et al (US 6,466,265).

Claim 24 is directed to a method for controlling power consumption in a CMOS active pixel sensor (APS) transducer array having a number of APS's arranged in columns and rows and connected to a power supply. The APS's can provide output signals representing an image however the outputs of selected APS's are not accessed to decimate the image thereby reducing the output bandwidth of the transducer array. The present method comprises the steps of determining the selected APS's having outputs that are not accessed and disconnecting the selected APS's from the power supply, thereby reducing the power consumption of the array.

Claims 25 to 30, which are directly or indirectly dependent on claim 24, further define the location of the selected APS's that are not being accessed.

As stated above, Wu does not discuss an image decimation technique, and further Wu does not teach a circuit that can connect and

disconnect selected APS's from between a power supply and ground thereby deenergizing selected APS's during the imaging process.

Lee teaches an APS sensor architecture which provides x-y addressability for sub-windowing and sub-sampling to limit the output bandwidth, however Lee does not teach a method of reducing power consumption by disconnecting the APS's that are not being accessed from the power supply.

In view of the above, it is therefore respectfully submitted that the teachings of Wu in view of Lee do not render claims 24 to 30 obvious to a person having ordinary skill in the art under 35 USC 103(a) and the Examiner is respectfully requested to withdraw his rejection of claims 24 to 30.

The prior art made of record by the Examiner includes:
US Patent 6,535,247 – Kozlowski et al which is directed to an APS with capacitorless correlated double sampling;
US Patent 6,549,234 – Lee which is directed to a pixel structure with an electronic shutter function; and
US Patent Publication 2002/0012057 – Kimura which is directed a drive method for a MOS sensor.

None of these documents teach a circuit for connecting and disconnecting selected APS's in an array from between a power supply and ground thereby deenergizing the selected APS's during the imaging process.

In view of the above amendments and remarks, and having dealt with all of the matters raised by the Examiner, early and favourable reconsideration of the application on its merits is respectfully requested.

If there are any further fees required by this communication, please charge such fees to our Deposit Account No. 16-0820, Order No. 33728.

Respectfully Submitted,

PEARNE & GORDON LLP

By _____
John P. Murtaugh, Reg. No. 34226

1801 East 9th Street
Suite 1200
Cleveland, Ohio 44114-3108
(216) 579-1700

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